IDEC Chip Design Contest

A Bio-Inspired Energy- and Area-Efficient Sound Localization Neural Network

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Abstract

An energy- and area-efficient sound localization neural network mimicking the auditory brainstem cognitive function is proposed. By adopting the bio-plausible Jeffress model, the proposed neural network locates the sound based on the interaural time difference (ITD) in an energy- and hardware-efficient manner. The proposed network modifies the original structure of the Jeffress model having a pair of long axon lines to reduce power consumption. Since only the leading pulse is allowed to propagate through the shortened single axon delay line, the number of delay elements and corresponding network components are reduced. A further reduction of the power consumption is achieved by eliminating redundant pulse propagation through the axon line after the output neuron fires. The proposed sound localization neural network was fabricated in a 28-nm CMOS process. The performance evaluation results indicate that the proposed sound localization neural network can detect the location of a sound source with a one-degree resolution at a given robot head size of 3.0125 cm, regardless of process corners. It also indicates that the network achieves up to 86.6% and 97.2% energy and area reduction from conventional sound localization networks, operating at 0.305-V supply voltage.

I. Introduction

Sound localization is an important auditory processing in the brainstem to coordinate the spatial origin of a sound source through the timing difference of sound signals received. Designing an accurate and energy-efficient sound localization system will be useful in applications such as speech recognition, robot navigation, and vehicle awareness [1]. However, previous sound localization systems using software or hardware implementations face limitations in power efficiency and computational complexity. This paper proposes a bio-inspired sound localization neural network which employs a single synchronized axon line with inhibitory behavior to reduce area and power consumption.

II. Proposed Sound Localization Neural Network

For energy-efficient sound localization neural network, the proposed sound localization neural network is designed by modifying the original Jeffress model architecture as shown in Fig. 1. In the proposed network, pulse generators transforming the sound inputs into pulses, a pulse selctor identifying the leading pulse, an axon line through which pulses are traveling, and NL neurons with spike inhibitors generating spikes indicating the angular position of the sound source are used. To minimize the power and hardware cost, an energy- and area-efficient CMOS neuron presented in [2] is used. Unlike the original Jeffress model, a single axon line is used thanks to the pulse selctor, which determines the direction of sound before the pulse is propagated through the axon line. Moreover, the axon line has a smaller number of delay elements (from 180 units to 90 units) compared to the original model. The use of a single axon line with half-length can reduce the total number of delay elements required to quarter, substantially reducing power and hardware cost. The number of NL neurons is also accordingly halved, leading to further power reduction. Moreover, the pulse stops propagating through the axon line after the firing of the winner neuron with the help of spike inhibitors, eliminating the power consumption due to redundant pulse propagation. Furthermore, due to digital implementation, the supply voltage can be scaled down such that the proposed sound localization neural network can operate in the subthreshold region, which brings additional power saving.

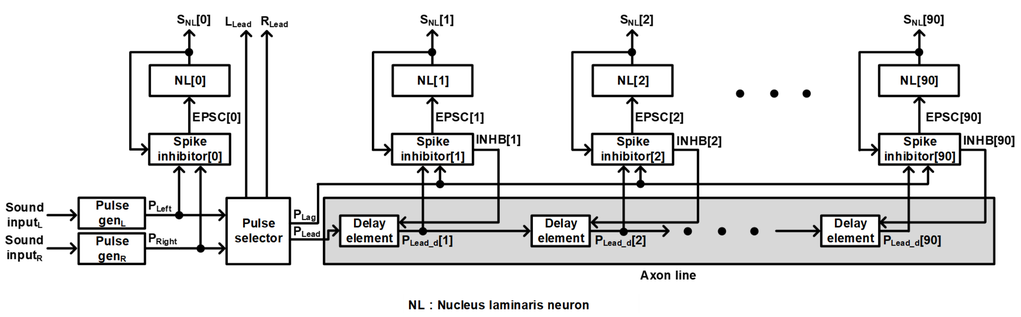
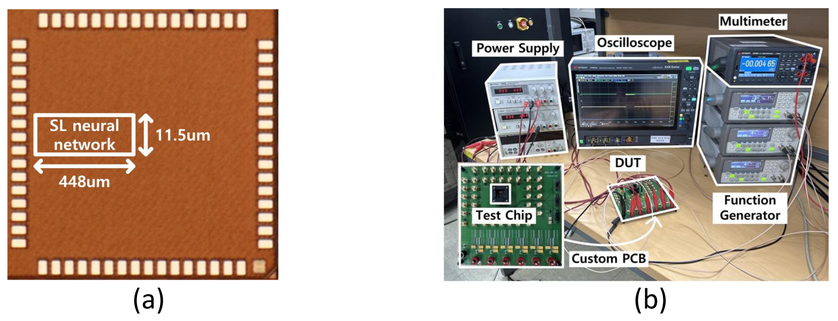


Fig. 1. Overall architecture of proposed sound localization neural network

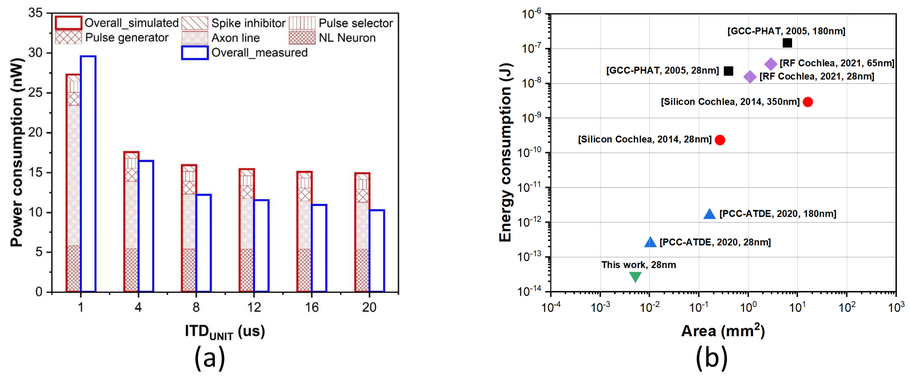
III. Measurements results

To investigate the feasibility and assess the performance, the proposed sound localization network was designed in a 28-nm CMOS process. The test chip has been fabricated, whose microphotograph and measurement setup are depicted in Fig. 2(a) and (b), respectively. The measured and simulated total power consumption versus unit ITD representing the head size of the robot adopting our network is presented in Fig. 3(a). The power consumption for unit ITD ranging from 1 to 20 μs (corresponding to head sizes from 3.0625 cm to 61.25 cm for one-degree resolution) is considered. The simulated total and component power consumptions are also depicted in the same figure for comparison, which shows good agreement with measured data. As expected, the amounts of power consumed by the axon line and NL neurons take up large portions of the overall power consumption. Along with smaller device counts, the internal signal transitions of the spike inhibitors, pulse selector, and pulse generator are rare, letting them consume relatively small amounts of power. To see this aspect in more detail, the energy consumption versus silicon area of various SL designs is depicted in Fig. 3(b). The improvements of the proposed design in terms of energy consumption and area originate from the adaptation of a bio-inspired model to avoid complex computations in conventional designs, and from the use of integrated circuit techniques to minimize hardware components and power consumption.



(a) (b)

Fig. 2. (a) Die microphotograph, (b) test environment for proposed sound localization neural network



(a) (b)

Fig. 3. (a) Simulated and measured power consumption versus unit ITD, (b) energy consumption versus silicon area of sound localization systems.

Acknowledgement

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Conclusions

This paper presents energy- and hardware-efficient sound localization architecture. It is designed in a 28-nm CMOS process, whose performance evaluation results indicate that the biologically plausible auditory system can be implemented in an energy- and area-efficient manner with a standard CMOS process, which envisions the practical realization of an energy-efficient bio-inspired system.

[1] S. Jeong et al., "21.6 A 12nW always-on acoustic sensing and object recognition microsystem using frequency-domain feature extraction and SVM classification," in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), San Francisco, CA, USA, Feb. 2017, pp. 362–363, doi: 10.1109/ISSCC.2017.7870411.

[2] B. Joo, J.-W. Han, and B.-S. Kong, "Energy- and area-efficient CMOS synapse and neuron for spiking neural networks with STDP learning," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 69, no. 9, pp. 3632–3642, Sep. 2022, doi: 10.1109/TCSI.2022.3178989.